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[Title of the Invention]

MANUFACTURING METHOD OF SEMICONDUCTOR APPARATUS

[Abstract]

[Problem] To provide a manufacturing method of a semiconductor apparatus in which an embedded wiring can be formed in an interlayer insulating film which comprises an organic material, without breaking down this interlayer insulating film.

[Means for Resolution] So as to cover a lower layer Al alloy wiring 3 which was formed on a Si substrate 1 through an interlayer insulating film 2, formed is an interlayer insulating film 4 which comprises an organic material with low dielectric constant such as fluorocarbon polymer, polyallylether fluoride, polyimide fluoride, polyparaxylylene. Next, after a connection hole 5 and a wiring groove 6 are formed in this interlayer insulating film 4, a TiN/Ti film 7 and a upper layer Al ally film 8 are sequentially formed on an entire surface of the Si substrate 1. Next, for example, at 420°C, reflow is applied to the upper layer Al alloy film 8 by use of a high pressure reflow method so as to fill in insides of the connection hole 5 and the wiring groove 6. After this, a unnecessary portion of TiN/Ti film 7 and upper layer Al alloy film 8 other than the connection hole 5 and the wiring groove 6 is removed by polishing to form a groove wiring which was embedded in the connection hole 5 and the wiring groove 6 and which was in contact with the lower layer Al alloy wiring 3.

[Claims]

[Claim 1] In a manufacturing method of a semiconductor apparatus which was configured in such a manner that an embedded wiring is formed in an interlayer insulating film which comprises an organic material,

a manufacturing method of a semiconductor apparatus characterized in that it is configured to form said embedded wiring by use of a high pressure reflow method.

[Claim 2] A manufacturing method of a semiconductor apparatus as set forth in Claim 1, characterized in that temperature at the time of embedding a wiring material for use in forming said embedded wiring by use of said high pressure reflow method is lower by at least 20°C than heat-resisting temperature of said organic material.

[Claim 3] A manufacturing method of a semiconductor apparatus as set forth in Claim 1, characterized in that a relative dielectric constant of said organic material is 3 or less.

[Claim 4] A manufacturing method of a semiconductor apparatus as set forth in Claim 1, characterized in that said organic material is fluorocarbon polymer, polyallylether fluoride, polyimide fluoride, polyparaxylylene.

[Claim 5] A manufacturing method of a semiconductor apparatus as set forth in Claim 4, characterized in that said fluorocarbon polyer is polytetrafluoroethylene.

[Claim 6] A manufacturing method of a semiconductor apparatus as set forth in Claim 1, characterized in that said embedded wiring comprises aluminum, copper, silver, gold or their alloy.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Belongs] This invention relates to a manufacturing method of a semiconductor apparatus, and in particular, is one which is preferable to be applied to manufacture of a semiconductor apparatus in which an embedded wiring is formed in an interlayer insulating film which comprises an organic material.

[0002]

[Prior Art] On the basis of requests of high integration, low power consumption and speeding up of semiconductor apparatuses, a low dielectric constant of an interlayer

insulating film which surrounds an internal wiring has become an important problem. As a low dielectric constant material which resolves this problem, at present, organic materials such as fluorocarbon polymer, polyimide fluoride, polyparaxylylene (parylene) have been studied. These organic materials realize low relative dielectric constant of approximately 2.0, by soaking carbon atoms (so-called alkyl group) so as to lower a density of a material and also to lower polarizability of molecules.

[0003] On one hand, in recent years, as a method which can realize miniaturization of a wiring and planarization of an interlayer insulating film by use of an easy-to-use process, a so-called groove wiring technology has been studied. This groove wiring is such a method that a predetermined wiring groove is formed in advance in an interlayer insulating film, and a film is formed over filling a wiring material such as Al alloy and Cu in an inside of this wiring groove, and polishing is carried out by a chemical mechanical polish (CMP) method, and a unnecessary portion of the wiring material which was deposited on a portion other than the wiring groove is removed to remain the wiring material only in the wiring groove, and this is used as a wiring.

[0004] In this groove wiring technology, among others, important is a technology for filling the wiring material well in a minute wiring groove. As a method thereof, a high temperature sputtering method of a wiring material such as Al alloy and Cu, a reflow method after sputtering, and so on have been studied. These high temperature sputtering method and reflow method are technologies which are based upon a sputtering method which has been used for forming a wiring up to now, and advantageous on points of its high productivity, stability, easy-to-use, and so on.

[0005] On this account, such a method that a wiring groove is formed in an interlayer insulating film which comprises above-described low dielectric constant organic material, and a wiring material is filled in this wiring groove by use of the high

temperature sputtering method and the reflow method and so on to form a groove wiring has promise as a method which can realize high integration and speeding up etc. of the semiconductor apparatuses at low cost.

[0006]

[Problem that the Invention is to Solve] However, in case that embedding of a wiring groove by use of the high temperature sputtering method and the reflow method etc. and an interlayer insulating film which comprises the above-described low dielectric constant material are combined, the following problems will occur. That is, in order to carry out embedding of a wiring materials such as Al alloy and Cu by use of the high temperature sputtering method and the reflow method etc., normally, required is high temperature heating with 500 to 550°C or more. On one hand, heat-resisting temperature of the above-described low dielectric constant organic material is generally approximately 450°C. On this account, there occurs such a problem that, by heating at the time of embedding of a wiring material by use of the high temperature sputtering method and the reflow method etc., an interlayer insulating film which comprises the low dielectric constant organic material is resolved, and broken down.

[0007] By the above-described reasons, such a technology has been desired that, even in case that an interlayer insulating film was formed by use of a low dielectric constant organic material such as fluorocarbon polymer in forming the embedded wiring, it is possible to fill a wiring material well in a wiring groove and to form an embedded wiring, without breaking down this interlayer insulating film.

[0008] Therefore, an objective of this invention is to provide a manufacturing method of a semiconductor apparatus which can form an embedded wiring in an interlayer insulating film which comprises an organic material, without breaking down

this interlayer insulating film.

[0009]

[Means for Solving the Problem] In order to accomplish the above-described objective, this invention is one which is characterized in that, in a manufacturing method of a semiconductor apparatus which was configured in such a manner that a embedded wiring is formed in an interlayer insulating film which comprises an organic material, it is configured in such a manner that the embedded wiring is formed by use of a high pressure reflow method.

[0010] In this invention, temperature at the time of embedding a wiring material for use in forming the embedded wiring by use of the high pressure reflow method is, preferably, selected to be lower by at least 20°C than heat-resisting temperature of the organic material which configures the interlayer insulating film.

[0011] In this invention, a relative dielectric constant of the organic material which configures the interlayer insulating film is typically 3 or less. AS the suchlike organic material, for example, cited are fluorocarbon polymer(relative dielectric constant 2.0), polyallylether fluoride(relative dielectric constant 2.5), polyimide fluoride(relative dielectric constant 2.6), polyparaxylene(relative dielectric constant 2.5) and so on. The fluorocarbon polyer is, to be more precise, for example, polytetrafluoroethylene. In this invention, the embedded wiring comprises, for example, aluminum(Al), copper(Cu), silver(Ag), Gold(Au) or their alloy.

[0012] In this invention, from a view point of preventing degasification from an interlayer insulating film at the time of high pressure reflow, and of improving a embedding characteristic of a wiring material, preferably, nitride processing is applied to a surface of an interlayer insulating film which comprises an organic material, and thereafter, an embedded wiring is formed.

[0013] According to a manufacturing method of a semiconductor apparatus by this invention, which was configured as described above, since it is possible to set process temperature at the time of high pressure reflow to be 450°C or less, even in case that an interlayer insulating film was formed by use of a low dielectric constant organic material whose heat-resisting temperature is approximately 450°C, it is possible to form an embedded wiring without breaking down this interlayer insulating film due to resolving etc.

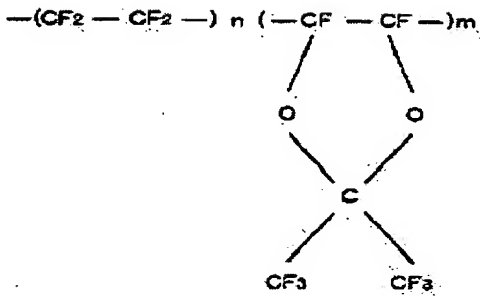
[0014]

[Mode for Carrying Out the Invention] Hereinafter, embodiments of this invention will be described with reference to drawings. In addition, in all figures of embodiments, the same reference numerals and signs are given to the same or corresponding portions.

[0015] Fig.1 to Fig.6 show a manufacturing method of a semiconductor apparatus by a first embodiment of this invention in the order of processes. In a manufacturing method of a semiconductor apparatus according to this first embodiment, firstly, as shown in Fig.1, on a Si substrate 1 on which devices (not shown) were formed in advance, formed is a lower layer Al alloy wiring 3 which comprises, for example, an Al alloy such as Al-0.5%Cu, through an interlayer insulating film 2 such as for example, SiO_2 film.

[0016] Next, as shown in Fig.2, on an entire surface of the Si substrate 1, formed is an interlayer insulating film 4 with film thickness of for example, 500nm, which comprises, for example, polytetrafluoroethylene represented by a chemical construction formula of

[Chemical Formula 1]



This film forming of the interlayer insulating film 4 which comprises polytetrafluoroethylene is, concretely speaking, carried out, for example, as follows. That is, firstly, this polytetrafluoroethylene is dissolved in fluorocarbon series solvent, and viscosity is adjusted to be 30cp, and thereafter, this is applied in a spinning manner on a substrate by use of a spin coater, to form a thin film with film thickness of 500nm. Spinning speed at this time is set to be, for example, 3000rpm. Successively, by use of N_2 gas which is inert gas, as ambient gas, baking (cure) is carried out for 2 minutes with conditions of 100°C and atmospheric pressure, to evaporate the solvent. In addition, as ambient gas for this baking, instead of N_2 gas, Ar gas, He gas etc. may be used. Next, for example, N_2 gas is used as ambient gas, and heat treatment is carried out with conditions of 300°C and atmospheric pressure, and the interlayer insulating film 4 is solidified.

[0017] Next, as shown in Fig.3, by use of a photolithography process and an etching process, formed are a connection hole 5 and a wiring groove 6 in the interlayer insulating film 4 at a portion above the lower layer Al alloy wiring 3. Any one of these connection hole 5 and wiring groove 6 may be formed in first.

[0018] Next, for example, by use of Ar sputter etching, removed is an oxide film (not shown) which was formed on a surface of the lower layer Al alloy wiring 3 at a bottom part of the connection hole 5. Next, as shown in Fig.4, for example, by use of a DC magnetron sputtering method, sequentially formed are a Ti film with film thickness of

e.g., 20nm and a TiN film with film thickness of e.g., 50nm to form a TiN/Ti film 7. Here, taking one example of sputtering conditions at the time of film forming of this Ti, Ar gas is used as process gas, and its flow volume is set to be 100sccm, and pressure is set to be 0.4Pa, and DC power is set to be 6kW, and substrate temperature is set to be 300°C. Also, taking one example of sputtering conditions at the time of film forming of this TiN film, mixed gas of Ar and N_2 is used as process gas, and their flow volumes are set to be 20sccm and 70sccm, respectively, and pressure is set to be 0.4Pa, and DC power is set to be 12kW, and substrate temperature is set to be 300°C.

[0019] Successively, by use of a DC magnetron sputtering method, on the TiN/Ti film 7, formed is a upper layer Al alloy film 8 with film thickness of e.g., 1μm which comprises, for example, Al-0.5%Cu alloy. At this time, this upper layer Al alloy film 8 is made to be of such a so-called bridge shape that voids are remained in insides of the connection hole 5 and the wiring groove 6. Taking one example of sputtering conditions at the time of film forming of this upper layer Al alloy film 8, Ar gas is used as process gas, and its flow volume is set to be 100sccm, and pressure is set to be 0.4Pa, and DC power is set to be 15kW, and substrate temperature is set to be 300°C.

[0020] Next, as shown in Fig.5, by use of a high pressure reflow method, reflow is applied to the upper layer Al alloy film 8, and insides of the connection hole 5 and the wiring groove 6 are filled with Al alloy, and also, surface planarization of the upper Al alloy film 8 is carried out. Taking one example of conditions of this high pressure reflow, Ar gas is used as process gas, and pressure is set to be $7X10^7$Pa, and reflow time is set to be 1 minute, and substrate temperature is set to be 420°C. Here, process temperature at the time of this high pressure reflow is 420°C as above, and is sufficiently lower than heat-resisting temperature (approximately 450°C) of the interlayer insulating film 4 which comprises polytetrafluoroethylene, and therefore, it

is possible to fill the upper layer Al alloy film 8, which is a wiring material, well in insides of the connection hole 5 and the wiring groove 6, by use of high pressure reflow. In addition, a series of processes from the above-described Ar sputter etching up to high pressure reflow are, preferably, carried out continuously in vacuum by use of a multiple chamber type processing apparatus.

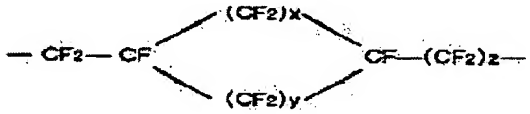
[0021] Next, for example, by use of a CMP method, polished and removed is unnecessary portions of the upper layer Al alloy film 8 and the TiN/Ti film 7 which were deposited on a portion other than the connection hole 5 and the wiring groove 6, and the upper layer Al alloy film 8 is remained in only insides of the connection hole 5 and the wiring groove 6. Taking one example of conditions of polishing by use of this CMP method, used is formed silica included slurry with the base of NH_4OH, and its flow volume is set to be 100cc/min, and polishing pressure is set to be $100g/cm^2$, and polishing temperature is set to be 25 to 30°C, and rotation speeds of both machine platen and polishing head are set to be 30rpm. By the foregoing, as shown in Fig.6, formed is a groove wiring 9 comprising Al alloy, which is embedded in the connection hole 5 and the wiring groove 6, and which was in contact with the lower layer Al alloy wiring 3.

[0022] As above, according to this first embodiment, in order to fill the upper layer Al alloy film 8 as a wiring material in insides of the connection hole 5 and the wiring groove 6, used is such a high pressure reflow method that process temperature is 420°C, sufficiently lower than heat-resisting temperature (approximately 450°C) of polytetrafluoroethylene which configures the interlayer insulating film 4, and therefore, it is possible to embed the upper Al alloy film 8 well in the insides of the connection hole 5 and the wiring groove 6, without inviting breakdown of this interlayer insulating film 4 due to resolving etc. And, by polishing this upper layer Al alloy film 8 by use

of the CMP method, it is possible to form the groove wiring 9 well. By the foregoing, it is possible to manufacture a semiconductor apparatus with high integration, low power consumption and high speed at low cost.

[0023] Next, a second embodiment of this invention will be described. In a manufacturing method of a semiconductor apparatus according to this second embodiment, in the same manner as in the first embodiment, everything up to the lower layer Al alloy wiring 3 was formed on the Si substrate 1, and thereafter, so as to cover this lower layer Al alloy wiring 3, formed is the interlayer insulating film 4 with film thickness of e.g., 500nm which comprises, for example, polytetrafluoroethylene represented by a chemical construction formula of

[Chemical Formula 2]



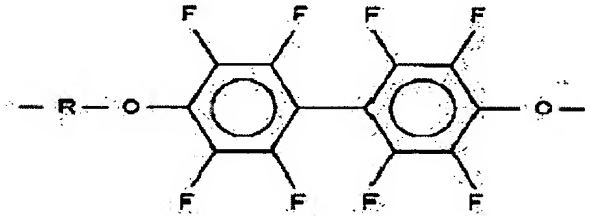
A film forming method of this interlayer insulating film 4 which comprises polytetrafluoroethylene is the same as in the first embodiment, except for such a fact that temperature of heat treatment for solidification which is carried out at the last is set to be 350°C. After this, in the same manner as in the first embodiment, processes after forming of the connection hole 5 and the wiring groove 6 are proceeded to form the groove wiring 9 comprising Al alloy, which is embedded in the connection hole 5 and the wiring groove 6, and which was in contact with the lower layer Al alloy wiring 3.

[0024] Even by this second embodiment, it is possible to obtain the same advantages as in the first embodiment.

[0025] Next, a third embodiment of this invention will be described. In a manufacturing method of a semiconductor apparatus according to this third

embodiment, in the same manner as in the first embodiment, everything up to the lower layer Al alloy wiring 3 was formed on the Si substrate 1, and thereafter, so as to cover this lower layer Al alloy wiring 3, formed is the interlayer insulating film 4 with film thickness of e.g., 500nm which comprises polyallylether fluoride polytetrafluoroethylene represented by a chemical construction formula of

[Chemical Formula 3]



A film forming method of this interlayer insulating film 4 which comprises polyallylether fluoride is the same as in the first embodiment, except for such a fact that temperature of heat treatment for solidification which is carried out at the last is set to be 350°C. After this, in the same manner as in the first embodiment, processes after forming of the connection hole 5 and the wiring groove 6 are proceeded to form the groove wiring 9 comprising Al alloy, which is embedded in the connection hole 5 and the wiring groove 6, and which was in contact with the lower layer Al alloy wiring 3.

[0026] Even by this third embodiment, it is possible to obtain the same advantages as in the first embodiment.

[0027] Next, a fourth embodiment of this invention will be described. In a manufacturing method of a semiconductor apparatus according to this fourth embodiment, in the same manner as in the first embodiment, everything up to the lower layer Al alloy wiring 3 was formed on the Si substrate 1, and thereafter, so as to cover this lower layer Al alloy wiring 3, formed is the interlayer insulating film 4 with

film thickness of e.g., 500nm which comprises, for example, polyimide fluoride (a thing in which a fluorocarbon material was mixed with polyimide). A film forming method of this interlayer insulating film 4 which comprises polyimide fluoride is the same as in the first embodiment, except for such a fact that temperature of heat treatment for solidification which is carried out at the last is set to be 350°C. After this, in the same manner as in the first embodiment, processes after forming of the connection hole 5 and the wiring groove 6 are proceeded to form the groove wiring 9 comprising Al alloy, which is embedded in the connection hole 5 and the wiring groove 6, and which was in contact with the lower layer Al alloy wiring 3.

[0028] Even by this fourth embodiment, it is possible to obtain the same advantages as in the first embodiment.

[0029] Next, a fifth embodiment of this invention will be described. In a manufacturing method of a semiconductor apparatus according to this fifth embodiment, in the same manner as in the first embodiment, everything up to the lower layer Al alloy wiring 3 was formed on the Si substrate 1, and thereafter, so as to cover this lower layer Al alloy wiring 3, formed is the interlayer insulating film 4 with film thickness of e.g., 500nm which comprises, for example, polyparaxylylene. For film forming of the interlayer insulating film 4 which comprises polyparaxylylene, used is a reduced pressure CVD method. The film forming by use of this reduced pressure CVD method is carried out, concretely speaking, in such a manner that, for example, diparaxylylene is used as a row material, and this row material is sublimated by heating it with 200°C, and this row material is resolved into xylylene monomer by heating it with 650°C along the way of transporting it on the Si substrate 1, and then, introduced on the Si substrate 1 with 150°C. After this, in the same manner as in the first embodiment, processes after forming of the connection hole 5 and the wiring

groove 6 are proceeded to form the groove wiring 9 comprising Al alloy, which is embedded in the connection hole 5 and the wiring groove 6, and which was in contact with the lower layer Al alloy wiring 3.

[0030] Even by this fifth embodiment, it is possible to obtain the same advantages as in the first embodiment.

[0031] Next, a sixth embodiment of this invention will be described. In a manufacturing method of a semiconductor apparatus according to the sixth embodiment of this invention, as shown in Fig.7, under such a situation that it was inserted in the midway of the interlayer insulating film 4 which comprises polytetrafluoroetylene in the same manner as in the first embodiment, formed is an etching stop layer 10 which comprises a material having etching resistance at the time of etching of the interlayer insulating film 4 such as a SiO_2 series film and a SiN film by use of for example, a plasma CVD method, and after that, formed is the connection hole 5 and the wiring groove 6 in the interlayer insulating film 4. At this time, at the time of etching so as to form the wiring groove 6, the etching stop layer 10 is used. After this, in the same manner as in the first embodiment, processes after forming of the TiN/Ti film 7 are proceeded to form the groove wiring 9 comprising Al alloy, which is embedded in the connection hole 5 and the wiring groove 6, and which was in contact with the lower layer Al alloy wiring 3.

[0032] According to this sixth embodiment, it is possible to obtain not only the same advantages as in the first embodiment but also such an advantage that it is possible to easily form the wiring groove 6 with a desired depth at favorable controllability, by the etching stop layer 10 which was formed in the midway of the interlayer insulating film 4.

[0033] Next, a seventh embodiment of this invention will be described. In a

manufacturing method of a semiconductor apparatus according to this seventh embodiment, as shown in Fig.8, in the same manner as in the first embodiment, the connection hole 5 and the wiring groove 6 were formed in the interlayer insulating film 4 which comprises polytetrafluoroetylene, and thereafter, a nitride layer 11 is formed by carrying out nitride processing of a surface of this interlayer insulating film 4. For this nitride processing, used is a plasma nitride method according to, for example, an electron cyclotron (ECR) method. Taking one example of conditions of this plasma nitride processing, mixed gas of H_2 and NH_3 and Ar is used as process gas, and their flow volumes are set to be 30sccm, 8sccm and 170sccm, respectively, and pressure is set to be 0.23Pa, and microwave power is set to be 2800W, and substrate temperature is set to be 400°C. In addition, instead of NH_3, N_2 may be used. After this, in the same manner as in the first embodiment, processes after forming of the TiN/Ti film 7 was proceeded to form the groove wiring 9 comprising Al alloy, which is embedded in the connection hole 5 and the wiring groove 6, and which was in contact with the lower layer Al alloy wiring 3.

[0034] According to this seventh embodiment, it is possible to obtain not only the same advantages as in the first embodiment but also such an advantage that, since the nitride layer 11 is formed on a surface of the interlayer insulating film 4 after the connection hole 5 and the wiring groove 6 were formed, it is possible to prevent degasification of moisture etc. from the interlayer insulating film 4 at the time of high pressure reflow which is carried out after that, and on this account, it is possible to more stabilize an embedding characteristic of the upper layer Al alloy film 8 due to high pressure reflow.

[0035] As above, embodiments of this invention were described concretely, but this invention is not one which is limited to the above-described embodiments and

available are a wide variety of modifications on the basis of a technical concept of this invention.

[0036] For example, film thickness, film forming conditions, high pressure reflow conditions, CMP conditions and so on which were taked in the above-described first to seventh embodiments are simply examples from first to last, and film thickness and conditions which are different from these may be used.

[0037] Also, instead of the TiN/Ti film 7 which was used in the above-described first to seventh embodiments, a Ti single layer film, a TiN single layer film, a Ti/TiN/Ti film and so on may be used. Furthermore, in case of film forming of these Ti film and TiN film, it is possible to use a CVD method. As this CVD method, concretely speaking, it is possible to use an ECR plasma CVD method, a thermal CVD method, a metalorganic chemical vapor deposition (MOCVD) method and so on.

[0038] Also, in the above-described first to seventh embodiment, Al-0.5%Cu was used as a wiring material but, as a wiring material, it is possible to use Al-Si, Al-Si-Cu, Ai-Ge and so on. Furthermore, in the above-described seventh embodiment, plasma nitride processing is carried out by use of the ECR plasma nitride method, but this plasma nitride processing may be carried out by a plasma nitride processing method which used an apparatus of a parallel flat plate system and of a magnetron system.

[0039] Also, in the above-described first embodiment, the lower layer Al alloy wiring 3 may be a groove wiring. Furthermore, in the above-described first to seventh embodiments, described was such a case that the groove wiring 9 as a upper wiring is made to be in contact with a top of the lower layer Al alloy wiring 3, but this invention is also applicable to such a case that the groove wiring 9 is made to be in contact with, for example, a diffusion layer formed in the Si substrate 1.

[0040]

[Advantage of the Invention] As described above, according to a manufacturing method of a semiconductor apparatus by this invention, it is configured in such a manner that an embedded wiring is formed by use of a high pressure reflow method, and therefore, it is possible to form an embedded wiring in an interlayer insulating film which comprises an organic material, without breaking down this interlayer insulating film.

[Brief Description of the Drawings]

[Fig.1] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to a first embodiment of this invention.

[Fig.2] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to the first embodiment of this invention.

[Fig.3] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to the first embodiment of this invention.

[Fig.4] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to the first embodiment of this invention.

[Fig.5] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to the first embodiment of this invention.

[Fig.6] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to the first embodiment of this invention.

[Fig.7] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to a sixth embodiment of this invention.

[Fig.8] is a cross sectional view for explaining a manufacturing method of a semiconductor apparatus according to a seventh embodiment of this invention.

[Description of Reference Numerals and Signs]

1...Si substrate, 3...lower layer Al alloy wiring, 4...interlayer insulating film,

5...connection hole, 6...wiring groove, 8...upper layer Al alloy film, 9...groove wiring, 10...etching stop layer, 11...nitride layer

[Fig.1]

3 LOWER LAYER Al ALLOY WIRING

2 INTERLAYER INSULATING FILM

1 Si SUBSTRATE

[Fig.2]

4 INTERLAYER INSULATING FILM

[Fig.3]

5 CONNECTION HOLE

6 WIRING GROOVE

[Fig.4]

8 UPPER LAYER Al ALLOY FILM

7 TiN/Ti FILM

[Fig.6]

9 GROOVE WIRING

[Fig.7]

10 ETCHING STOP LAYER

[Fig.8]

11 NITRIDE LAYER